LISTING OF CLAIMS

Claims 1-17 (canceled)

18. (currently amended) A method of forming a memory integrated circuit comprising:

forming a plurality of delay elements on a substrate of a random access memory integrated circuit, each delay element of said plurality including an input and output;

coupling said respective inputs and outputs of said delay elements to one another to form a delay line having a first one and a last one of said plurality of delay elements;

forming a switching device on said substrate;

coupling an input of said first delay element to an output of said switching device;

forming a clock input terminal of said random access memory integrated circuit on said substrate;

coupling a first clock input of said switching device to said clock input terminal;

forming a mode-control input terminal of said random access memory integrated circuit on said substrate; and

coupling a second control input of said switching device to said mode-control input terminal, said mode-control input terminal being [[input]] adapted to receive a power-up/power-down signal signifying a power-up/power-down mode of said memory integrated circuit.

19. (previously presented) A method of forming a memory integrated circuit as defined in claim 18 further comprising:

forming an electric power input terminal on said substrate; and

coupling each said delay element to said electrical power input terminal, said plurality of delay elements being adapted to draw a first quantity of power through said electric power input terminal during a first time interval and a second quantity of power through said electric power input terminal during a second time interval, said second quantity of power being greater than said first quantity of power, said second time interval corresponding to a power-up state of said power-up/power-down signal.

20. (currently amended) A method of operating a memory integrated circuit comprising:

switchingly controlling an application of a periodic clock signal to an input node of a delay line of a delay locked loop of said memory integrated circuit, whereby during a first time interval, in which said memory integrated circuit is in a power-up mode, an output signal of said delay locked loop ~~cycles~~ alternates and during a second time interval, in which said memory integrated circuit is in a power-down mode, said output signal of said delay locked loop ~~is static~~ does not alternate.

21. (previously presented) A method of operating a memory integrated circuit defined in claim 20 further comprising:

coupling said delay line to an electrical power supply;

receiving a first quantity of power from said electrical power supply during said first time interval;

receiving a second quantity of power from said electrical power supply during said second time interval, said first quantity of electrical power being greater than said second quantity of electrical power.

22. (previously presented) A method of operating a memory integrated circuit defined in claim 21 wherein conservation of power produced by said electrical power supply is functionally related to a ratio of lengths of said first time interval and said second time interval.

23. (previously presented) A method of operating a memory integrated circuit as defined in claim 20 further comprising:

switching a transistor having an output coupled to an input of said delay line at a time between said first time interval and said second time interval.

24. (previously presented) A method of operating a memory integrated circuit as defined in claim 20 further comprising:

dissipating a first amount of power from said delay line during said first time interval; and

dissipating a second amount of power from said delay line during said second time interval, said first amount of power being greater than said second amount of power.

25. (previously presented) A method of operating a memory integrated circuit as defined in claim 20 further comprising:

receiving said periodic clock signal at said memory integrated circuit from a clock source external to said memory integrated circuit during both said first and second time intervals.

26. (previously presented) A method of operating a memory integrated circuit comprising:

the step of receiving a periodic clock signal at an input of a delay locked loop delay line during a first time interval; and

the step of receiving a DC signal at said input of said delay locked loop delay line during a second time interval, whereby less power is dissipated from said delay locked loop delay line during said second time interval than during said first time interval.

27. (previously presented) A method of operating a memory integrated circuit as defined in claim 26 wherein said DC signal comprises a ground potential signal.

28. (previously presented) A method of operating a memory integrated circuit as defined in claim 26 further comprising:

the step of receiving a periodic clock signal at a clock input of said memory integrated circuit during both said first time interval and said second time interval.

29. (previously presented) A method of operating memory integrated circuit as defined in claim 28 further comprising:

the step of dissipating a quantity of power related to each toggle of said sequentially toggling.

30. (previously presented) A method of operating a memory integrated circuit as defined in claim 26 further comprising:

the step of sequentially toggling a plurality of delay elements within said delay locked loop delay line during said first time interval, said delay elements being coupled in series with one another.

31. (currently amended) A clock signal received at an output of a delay line, said clock signal comprising:

a first signal portion having a periodic signal characteristic, said first signal portion being present during a first ~~power-up~~ time interval signifying a power-up mode of a

memory integrated circuit including said delay line and when a periodic input waveform is received at an input of said delay line; and

a second signal portion having a DC signal characteristic, said second signal portion being present during a second ~~power-down~~ time interval signifying a power-down mode of said memory integrated circuit and when a DC input waveform is received at said input of said delay line.

32. (previously presented) A clock signal received at an output of a delay line as defined in claim 31 wherein said periodic waveform and said the DC waveform are received from a switching device during said first and second time intervals respectively.

33. (previously presented) A clock signal received at an output of a delay line as defined in claim 31 wherein a power dissipation in said delay line during said first power-up time interval exceeds a power dissipation in said delay line during said second power-down time interval.

34. (currently amended) A memory integrated circuit device comprising:

memory logic array; and

a delay locked loop circuit, said delay locked loop circuit including a delay line having an input and an output; and

controlling means for controlling an externally generated periodic clock signal depending upon whether said memory integrated circuit device is in a power-up mode or a power-down mode, said controlling means coupled to said input of said delay line.

35. (previously presented) A memory integrated circuit device as defined in claim 34 wherein said controlling means comprises:

a transistor adapted to alternately block and pass said externally generated periodic clock signal.

36. (previously presented) A memory integrated circuit device as defined in claim 34 further comprising:

an external clock input adapted to be coupled to a source of an externally generated clock signal, said external clock input being electrically coupled to an input of said controlling means.

37. (previously presented) A memory integrated circuit device as defined in claim 34 wherein said delay line comprises a plurality of delay elements coupled in series with one another, said plurality of delay elements being adapted to dissipate a first amount of power in response to receiving said periodic clock signal and being adapted to dissipate a second smaller amount of power in response to receiving no clock signal.